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2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **HASHIMOTO, Hiroshi et al.**

Group Art Unit: **2814**

Serial No.: **09/960,399**

Examiner: **Howard Weiss**

Filed: **September 24, 2001**

P.T.O. Confirmation No.: **5652**

For: **A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS (as amended)**

REQUEST FOR RECONSIDERATION UNDER 37 CFR §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 31, 2003

Sir:

In response to the Office Action dated **May 2, 2003**, please amend the above-identified application as follows: